Computer Architecture

Leo and Jeff

Architecture is…

- **High Level** processor / ISA design
- Cores galore!
- Interconnects
- Memory
- Exploiting parallelism

- Who's hot?

Big Players (Domestic)

- U Wisconsin - Madison
- Berkeley
- Stanford
- UIUC
- U Michigan – Ann Arbor
- UW
- UCSD

- What's hot?

Traditional Architecture

- Caching
- Prefetching
- Branch Prediction
- Speculation
- Pipelining

(Everyone does these)

Power!

- **At least** as important as performance
- Soon - can’t turn on the whole chip
  - App. specific hardware
- Off chip power
- Mobile

- UCSD: Arsenal (Swanson/Taylor), Adaptive power (Tullsen/VK), McPAT (Tullsen/Rick), Rosing

Parallelism

- Instruction Level
- Thread Level
- Inter-core
- ISA (punt)

- UCSD – SMT (Tullsen), Thread Migration (Tullsen/Jeff)
- Others: Berkeley “Seven Dwarves”, Stanford, UIUC, (everyone!)

Transactional Memory

- Simpler Parallel Programming
- Opportunistic Concurrency

- UCSD: PTM (Jack, Ganesh), SpMT (Tullsen/Leo)
- Others: Bulk (UIUC), TCC (Stanford)

Interconnect

- On-chip networks
- Trend: point-to-point
- Synchronization

- UIUC (Sarita, Rakesh), Stanford (Dally)

Memory Systems

- New devices
  - Flash, **Phase Change**, etc.
- Reliability

UCSD – Flash Gordon (Swanson's folks), Rosing

Misc

- Support for security, debugging…
- Reliability / Devices
  - Useful boundary with device guys
  - Driven by power and feature size
- Programming Languages (HELP?!)
  - Parallelism defined / hints

UCSD: Thermal Reliability(Rick, Ayse); Simpoint (Calder, Sherwood)